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TRANSMITTAL FORM

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Application Number	09/476,622
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First Named Inventor	Howard Chin
Art Unit	2183
Examiner Name	William M. Treat
Total Number of Pages in This Submission: 87	Attorney Docket Number: 42390.P6746

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
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- ☐ After Allowance communication to Technology Center (TC)
- ☑ Appeal Communication to Board of Appeals and Interferences *
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) (please Identify below):

Remarks

*Appeal Brief in triplicate is enclosed.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Dennis A. Nicholls Reg. No. 42,036
Signature	
Date	October 15, 2004

CERTIFICATE OF TRANSMISSION/MAILING

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Typed or printed name	Anne Collette		
Signature	Anne Collette	Date	October 15, 2004

Docket No.: 42390.P6746

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re the application of:	)	
	)	
Chin, Howard, et al.	)	
	)	
Serial No.: 09/476,622	)	Examiner: Treet, W. M.
	)	
Filed: 12/31/1999	)	Art Unit: 2183
	)	
For: EXTERNAL MICROCODE	)	

APPELLANTS' BRIEF UNDER 37 CFR § 1.192
IN SUPPORT OF APPELLANTS' APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES (REVISED)

Hon. Commissioner for Patents
Mail Stop Appeal Brief – Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants hereby submit this Brief in triplicate in support of an appeal from a final decision of the Examiner, in the above-referenced case. Appellants respectfully request consideration of this appeal by the Board of Patent Appeals and Interference for allowance of the above-referenced patent application.

TABLE OF CONTENTS

I. Real Party in Interest

The real party in interest in the present appeal is Intel Corporation, a Delaware Corporation headquartered in Santa Clara, California, the assignee of the present application.

II. Related Appeals and Interferences

There are no related appeals or interferences to appellants' knowledge that would have a bearing on any decision of the Board of Patent Appeals and Interferences.

III. Status of the Claims

Claims 1 through 20 and 22 through 28 are cancelled.

Claims 21 and 29 through 40 are pending in the application.

Claim 38 stands rejected under 35 U.S.C. 103(a) over Shiraogawa et al. (U.S. Patent No. 4,131,943, hereinafter *Shiraogawa*) and matter officially noticed. Claims 21, 29 through 34, and 38 through 40 stand rejected under 35 U.S.C 102(e) over Mahalingaiah et al. (U.S. Patent No. 6,141,740, hereinafter *Mahalingaiah*) in light of Witt (U.S. Patent No. 5,623,619, hereinafter *Witt*). Claims 21, 35, and 36 stand rejected under 35 U.S.C. 102(b) over Dao et al. (U.S. Patent No. 4,928,223, hereinafter *Dao*). Claim 37 stands rejected under 35 U.S.C. 103(a) over *Dao* and

matter officially noticed. Claim 37 further stands rejected under 35 U.S.C. 112, first paragraph.

Claims 21 and 29 through 40 are the claims presently under this appeal.

IV. Status of Amendments

Appellants submitted an amendment after final which was mailed 12/17/2003. An Advisory Action was mailed on 01/29/2004 which stated that the request for reconsideration had been considered but that it did not place the application in a condition for allowance.

Appellants submitted on 04/21/2004, concurrent with the initial Appeal Brief, an amendment after final rejection under 37 CFR 1.116(b). Appellants submitted that this amendment merely canceled claim 10, and corrected typographic errors in claim numbering, and therefore placed the application in better form for appeal.

A Notification of Non-compliance with 37 CFR 1.192(c) was mailed on 09/15/2004, stating that the initial Appeal Brief did not contain a correct copy of the appealed claims, and furthermore that the amendment after final submitted 04/21/2004 had not been entered.

Appellants submit, concurrent with the present revised Appeal Brief, a new amendment after final rejection under 37 CFR 1.116(b) which only cancels claims. These claims are reproduced in clean form in the appendix of the present revised Appeal Brief.

V. Summary of the Invention

Appellants' disclosure describes a method and apparatus for utilizing microcode stored externally to a processor. In one embodiment, the disclosure describes how firmware code, including microcode instructions, which resides externally to the processor may be used as microcode by using machine specific registers (MSRs) as the interface. "The bits stored by the MRSs 208 are updated when the firmware code 210 stored in the firmware 206 is executed by the processor 204." (Specification page 5, lines 9 – 11, and Figure 2A.)

The firmware code, brought in via the *normal instruction path* and executed by the processor, may act to move microcode, originally placed into a general-purpose register, into a machine specific register.

> In one embodiment, the data control unit 310 fetches an instruction from memory or from firmware or from any other computer readable medium external to the processor. The data control unit 310 then decodes the instruction into one or more operations known as microinstructions. In one embodiment, logical source and destination registers for each microinstruction are general purpose registers. According to one embodiment of the present invention, the logical source or destination register for some of the microinstructions fetched from the firmware is one of the machine specific registers such as the MSR 314 for functional unit E 308e.

(Specification page 6, lines 16 – 24, and Figure 3.) In this manner the microcode is loaded into the machine specific register where it may be directly used as microcode, without any special data or address paths being added to the external interface of the processor.

VI. Issues

1. Whether claim 38 is unpatentable under 35 U.S.C. 103(a) over Shiraogawa et al. (U.S. Patent No. 4,131,943) and matter officially noticed.

2. Whether claims 21, 29 through 34, and 38 through 40 are unpatentable under 35 U.S.C 102(e) over Mahalingaiah et al. (U.S. Patent No. 6,141,740) in light of Witt (U.S. Patent No. 5,623,619).

3. Whether claims 21, 35, and 36 are unpatentable under 35 U.S.C. 102(b) over Dao et al. (U.S. Patent No. 4,928,223), including whether claim 37 is unpatentable under 35 U.S.C. 103(a) over Dao et al. and matter officially noticed.

4. Whether claim 37 is unpatentable under 35 U.S.C. 112, first paragraph as failing to comply with the written description requirement.

VII. Grouping of Claims (Independent Claims **Bolded**)

With regards issue 1, claim **38** is under appeal.

With regards issue 2, claims **21**, **29**, 30 through 34, and **38** through 40 are under appeal.

With regards issue 3, claims **21**, **35**, 36, and 37 are under appeal.

With regards issue 4, claim 37 is under appeal.

VIII. Argument

A. Claim 38 Is Not Obvious In View Of Shiraogawa Et Al. And Matter Officially Noticed.

Claim 38 stands rejected under 35 U.S.C. 103(a) over Shiraogawa (U.S. Patent No. 4,131,943, hereinafter *Shiraogawa*) and matter Officially Noticed.

To establish a *prima facie* case of obviousness, case law as cited in the MPEP requires three criteria.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure.

In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991), cited in MPEP section 706.02(j).

Moreover, the Federal Circuit has recently cautioned that the Patent Office must support its rejections for reasons that are stated on the record that establish why a particular combination would have been motivated by the prior art. It is inadequate to just state in conclusory

fashion that just because two elements existed in the prior art, that someone should have or would have been motivated to combine them. A specific teaching or a specific principle must be stated that makes the combination obvious.

> The need for specificity pervades this authority. See, e.g., In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed"); In re Rouffet, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("even when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references").

In re Sang Su Lee, 277 F.3d 1338, 61 USPQ 1430 (Fed. Cir. 2002).

Appellants submit that (a) no specific showing of motivation to combine the references has been provided, and (b) that the references, even if combined, do not provide the claimed invention. Appellants further submit (c) that the matter Officially Noticed is not proper.

a. No Specific Showing of Motivation to Combine

The contention in the Final Office Action that it would be obvious

to combine *Shiraogawa* and matter Officially Noticed is both factually and legally erroneous.

i. Factually, *Shiraogawa* Does Not Suggest

Shiraogawa teaches a traditional-architecture microcoded processor, wherein a decode DROM 12 decodes an instruction and recovers associated microcode from a microcode ROM 15. The individual instructions coming from instruction register 11 cannot change any microcode stored in ROM 15. In contrast, present claim 38 recites in pertinent part "a selected one of the at least two machine specific register is updated in response to *executing* a microcode instruction fetched from a memory external to the processor." Any microcode brought into the *Shiraogawa* architecture would require an extension of address and data busses used for accessing ROM 15 off the processor, which would require considerable extra pins or a complicated multiplexing scheme. Hence there is no *intrinsic* teaching that storing an instruction off-processor would be useful for changing the microcode.

The entirety of the explanation from the Office Action of why a "macroinstruction/machine-instruction programs in external memory" should be added to *Shiraogawa* reads as follows:

> One of ordinary skill is motivated to store such programs externally to conserve valuable internal chip real estate.

Final Office Action dated 10/22/2003, paragraph 7.

The Office Action makes no explanation whatsoever as to why the externally stored macroinstructions would be useful when added to the computer of *Shiraogawa*. As mentioned above, modifying the microcode in ROM 15 by the *execution* of any instructions is not discussed in *Shiraogawa*, hence there is no intrinsic teaching that such enhancements would be useful.

ii. Legally, Burden Not Met

Furthermore, appellants submit that the evidentiary burden for an obviousness rejection has not been met. The Federal Circuit was specific in its admonitions in *In re Sang Su Lee*, quoted above. Particular factual findings are required to underpin a section 103 rejection. Here, the Final Office Action only makes the conclusory statement that "[o]ne of ordinary skill is motivated to store such programs externally to conserve valuable internal chip real estate."

No factual basis is given as to why someone would be motivated to add modifications to the computer of *Shiraogawa*, particularly in view of the fact that *Shiraogawa* did not use the instruction from instruction register 11 to make any changes to the contents of microcode ROM 15. What is the motivating factor to use the Officially Noticed storage of *macroinstructions* in an external media, as this would not cause any

microcode changes? Without an evidentiary basis upon which to draw this conclusion, the conclusion cannot stand.

b. Even If Combined, *Shiraogawa*, and The Matter Officially Noticed, Do Not Meet the Claim Limitations

As discussed above, appellants submit that insufficient motivation exists to combine the *Shiraogawa* reference with the matter Officially NOticed. Even assuming, however, that such a combination is made, the combination itself does not include all of the elements and limitations of appellants' claims.

Claim 38 stands rejected as being anticipated by *Shiraogawa* and the matter Officially Noticed. The computer of *Shiraogawa* discloses no "selected one of the at least two machine specific register is updated in response to executing a microcode instruction fetched from a memory external to the processor" as recited in pertinent part in claim 38. Instead, the computer of *Shiraogawa* merely *accesses* microcode stored in ROM 15, and does not *update* it. Indeed there are no "microcode instructions" of the present disclosure, capable of modifying microcode, disclosed either in *Shiraogawa* or in the matter Officially Noticed.

Appellants submit that *Shiraogawa* and matter Officially Noticed considered together do not disclose all of the claim elements and limitations of present claim 38. Therefore appellants submit that the

invention claimed in claim 38 is not anticipated by *Shiraogawa* and matter Officially Noticed, and therefore that claim 38 is allowable over the prior art of record.

c. Examiner Has Not Produced An Affidavit As Required Under 37 C.F.R 1.104(d)(2)

The Final Office Action, at paragraph 7, "takes Official Notice of the fact that storage of macroinstruction/machine-instruction programs in external media is well known in the art. One of ordinary skill is motivated to store such programs externally to conserve valuable internal chip real estate." However, these bare assertions are unsupported by evidence in the record, and in fact are negated by the showing above that the matter cited as Officially Noticed does not demonstrate the precise type of external storage claimed by appellants.

Actual microcode ready for access by the decode ROM 12 of *Shiraogawa* is not part of the matter Officially Noticed: neither is the use of a "microcode instruction fetched from a memory external to the processor" as recited in claim 38. All that was Officially Noticed is the external storage of traditional macroinstructions, and this does not support a finding of obviousness.

Therefore appellants believe they have successfully traversed the matter Officially Noticed, and, as discussed in depth in MPEP section 2144.03(C), the Examiner is respectfully requested to submit an affidavit

as required by 37 C.F.R. § 1.104(d)(2). Appellants point out that such a request for an affidavit was made in the previous Response under 37 C.F.R 1. 116, mailed 12/17/2003, at page 11.

Appellants respectfully submit that all the claim elements and limitations of claim 38 are not disclosed in the combined *Shiraogawa* reference and the matter Officially Noticed. Therefore appellants submit that a proper *prima facie* case of obviousness has not been made out in the Office Action mailed 10/22/2003. Appellants therefore submit that claim 38 is patentable over the *Shiraogawa* reference and the matter Officially Noticed.

B. Claims 21, 29 Through 34, And 38 Through 40 Are Not Anticipated By Mahalingaiah et al. in light of Witt.

Claims 21, 29 through 34, and 38 through 40 stand rejected under 35 U.S.C 102(e) over Mahalingaiah et al. (U.S. Patent No. 6,141,740, hereinafter *Mahalingaiah*) in light of Witt (U.S. Patent No. 5,623,619, hereinafter *Witt*).

The Final Office Action of 10/22/2003, at paragraph 11, recites

the following as its *entire argument* on this issue:

> Based on applicants strong arguments that a register associated with a functional unit is a machine specific register the examiner is interpreting the registers inherent in the reservation stations (22), the registers inherent in the reorder buffer (32), etc. as machine specific registers as well as the patch data registers (col. 16, lines 49 – 60). Witt, which is incorporated by reference in Mahalingaiah, accounts for the presence of a cache line valid bit (col. 8, lines 23 – 37) in Mahalingaiah.

Nothing else in the Final Office Action purports to explain the relevance of *Mahalingaiah* to the claimed invention. Furthermore, combining the *Witt* reference to *Mahalingaiah* does not appear to be proper under 35 U.S.C. 102(e), even if it is "incorporated by reference", although it could theoretically be proper when used in a 35 U.S.C 103 rejection. Appellants wish to point out that *Mahalingaiah* was first listed as a reference in the Office Action mailed on 09/27/2001, but no arguments based on *Mahalingaiah* were presented until the present Final Office Action. Hence the above-cited argument is the only argument which has been presented in the prosecution history of the present application to date.

Anticipation under 35 U.S.C. 102 requires the disclosure in a single prior art reference of each element of the claim under consideration. *See Verdegaal Bros. V. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). It is not enough,

however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

Appellants fail to see each element and limitation of claims 21, 29 through 34, and 38 through 40 in *Mahalingaiah*. As the Office Action has not presented any correspondences between *all of the elements and limitations of claims 21, 29 through 34, and 38 through 40* and matter disclosed in *Mahalingaiah*, appellants submit that the rejection under 35 U.S.C 102(e) of claims 21, 29 through 34, and 38 through 40 is improper and should be withdrawn. Appellants submit that claims 21, 29 through 34, and 38 through 40 are patentable over the cited *Mahalingaiah* and *Witt* references.

C. Claims 21, 35, And 36 Are Not Anticipated By Dao et al., And Futhermore Claim 37 Is Not Obvious In View Dao et al. And Matter Officially Noticed.

Claims 21, 35, and 36 stand rejected under 35 U.S.C. 102(b) over Dao et al. (U.S. Patent No. 4,928,223, hereinafter *Dao*). Claim 37 stands rejected under 35 U.S.C. 103(a) over *Dao* and matter officially noticed.

The Final Office Action of 10/22/2003, at paragraph 14, recites the following as its *entire argument* on this issue in regards claims 21, 35, and 36:

> Based on applicants strong arguments that a register associated with a functional unit is a machine specific register the examiner is interpreting the registers such as the exponent registers (150), instruction register (106), nano instruction registers (3038, 3040), status word register (Fig. 17), control word register (Fig. 18), etc. as machine specific registers.

Nothing else in the Final Office Action purports to explain the relevance of *Dao* to the claimed invention of claims 21, 35, and 36.

Anticipation under 35 U.S.C. 102 requires the disclosure in a single prior art reference of each element of the claim under consideration. *See Verdegaal Bros. V. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). It is not enough, however, that the prior art reference discloses all the claimed elements in

isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

Appellants fail to see each element and limitation of claims 21, 35, and 36 reflected in *Dao*. As the Office Action has not presented any arguments purporting to establish correspondences between *all of the elements and limitations of claims* 21, 35, and 36 and matter disclosed in *Dao*, appellants submit that the rejection under 35 U.S.C 102(b) of claims 21, 35, and 36 is improper and should be withdrawn.

Appellants have in good faith followed the suggestion in a previous Office Action, mailed 09/27, 2001, to read *Dao* column 24, line 37, through column 27, line 3 in regards other claims currently cancelled. From this reading, appellants believe that *Dao* does not define microcode in the same way as the appellants. *Dao* teaches the existence of macrocode, microcode, and nanocode. (*Dao*, column 1, line 63 through column 2, line 8.) While the existence of an external microcode read only

memory (ROM) 3000 is noted, it has its own local bus (3018, 3020). "The external microcode ROM 3000 has its own address and data bus, independent of the main CPU bus." (*Dao* column 25, lines 49 and 50.) Pending claim 21 recites in pertinent part "a computer readable medium external to the processor and coupled to the processor by the bus, the computer readable medium to store *instructions to implement microcode functions.*" The ROM 3000 of *Dao* does not store instructions to implement microcode functions, rather it stores the microcode itself directly, and clearly the local bus 3018, 3020 does not convey instructions. Hence the ROM 3000 and local bus 3018, 3020 of *Dao* cannot be the bus and computer readable medium recited in pending claim 21.

Similarly, pending claim 35 recites in pertinent part "storing microcode in firmware external to a processor; *executing the microcode* by the processor." The ROM 3000 of *Dao* does not store microcode which is *executed* by the processor to implement microcode functions: instead, it stores the microcode itself directly.

Furthermore, it is noted that the microcode of *Dao* merely defines the starting point of a nanocode instruction sequence. (*Dao* at column 35, lines 19 through 21.) The arithmetic logic unit (ALU) handles nanocode sequencing, and not microcode sequencing. (*Dao* at column. 37, lines 42 through 55.) Thus, it is the "nanocode" instructions of *Dao*

which equate to the terms "microcode" functions and "programmed code" used by appellants, and these nanocode instructions of *Dao* are not stored in external memory, but in a ROM and a programmable logic array integral with the ALU. (*Dao*, Figs. 2 and 15, and Col. 7, lines 3 through 25.)

For all these reasons appellants submit that claims 21 and 35 are patentable over the cited *Dao* reference. Since dependent claims 36 and 37 depend from independent claim 35, appellants further submit that all claims 21, 35, 36, and 37 are patentable over the *Dao* reference.

The Final Office Action of 10/22/2003, at paragraph 14, recites the following as its *entire supplemental argument* on this issue in regards claim 37:

> Dao taught the invention of claim 35 (paragraphs 13 – 14, supra) from which claim 37 depends. Also, while Dao taught external microcode and even the importance of being able to modify the external microcode, he did not specifically teach the processor modifying the microcode in firmware nor did the applicant's original disclosure for that matter. Dao taught modification of the code in RAM. However, the examiner takes Official Notice of the fact that firmware storage that is readily modifiable by a processor was prevalent at the time of applicants' invention. Dao would have been motivated to use it to store and revise his microcode because it is readily modifiable given the frequency with which one typically modifies microcode but is also relative secure from tampering by the

incompetent.

However, these bare assertions are unsupported by evidence in the record. Claim 37 recites in pertinent part "reprogramming the microcode in the firmware." The purportedly "firmware storage that is readily modifiable by a processor" which was Officially Noticed does not by itself disclose any "reprogramming the microcode in the firmware", where "the microcode" and "the firmware" have the meanings recited in independent claim 35. All that was Officially Noticed is the external storage of firmware that may be modified, and this does not support a finding of obviousness.

Therefore appellants believe they have successfully traversed the matter Officially Noticed, and, as discussed in depth in MPEP section 2144.03(C), the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2). Appellants point out that such a request for an affidavit was made in the previous Response under 37 C.F.R 1. 116, mailed 12/17/2003, at page 12.

Appellants reiterate that, since dependent claim 37 depends from independent claim 35, claim 37 is patentable over the *Dao* reference and the matter Officially Noticed.

D. Claim 37 Does Comply With The Written Description

Requirement Of 35 U.S.C. 112, First Paragraph.

Claim 37 stands rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The Final Office Action of 10/22/2003, at paragraph 14, recites the following.

> Applicants' claim 37 now claims that the processor modifies the external microcode firmware where previously the firmware was only modified without the agent of change being identified. While the examiner might readily acknowledge any idiot in the art might have the knowledge and motivation to use the processor and something like EEPROM to modify the external microcode, this has never been part of applicants' written disclosure prior to this time and constitutes new matter.

Appellants wish to point out the following quotation from the present specification *as originally filed*:

> By using microcode that is stored outside the processor, the cost of implementing microcode is significantly reduced because the code size restriction for the microcode is removed. External microcode according to one embodiment of the invention can also be reprogrammed easily and therefore increases the ease of debugging microcode. The ability to reprogram also makes errata fixes possible, much like a software patch, even after a processor is out in the market. Embodiments of the invention overcome the traditional requirement that microcode is so tightly coupled to the processor logic that the microcode must to be placed on the processor die.

Present specification at page 8, lines 23 through 30.

Furthermore, appellants wish to point out that currently-cancelled claim 17 *as originally filed* recites "[t]he method of claim 15 further comprising reprogramming the programmed code in the firmware."

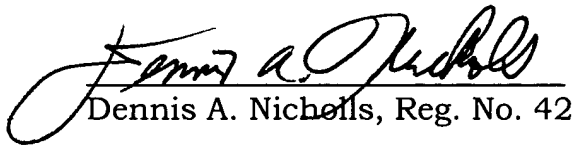
Appellants submit that these recitations in the specification and claims as originally filed fulfill the written description requirements of 35 U.S.C. 112, first paragraph. Appellants submit that pending claim 37 does not recite new matter, as the matter of pending claim 37 is clearly discussed in the above quotations from the specification and claims as originally filed. Therefore, appellants respectfully submit that the rejection of claim 37 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement, should be withdrawn.

Conclusion

Appellants respectfully submit that all claims now pending are in condition for allowance. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Acct. No. 02-2666.

Respectfully submitted,

Date: October 15, 2004



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IX. Appendix A: Claims Involved in Appeal (Clean Copy)

Claims 1 - 20. (Canceled)

21. (Previously presented) A system, comprising:

a bus;

a processor including a plurality of machine specific registers, wherein each one of the plurality of machine specific registers is associated with one or more functional units of the processor; and

a computer readable medium external to the processor and coupled to the processor by the bus, the computer readable medium to store instructions to implement microcode functions which result in changing a value of at least one bit in at least one of the plurality of machine specific registers.

Claims 22 - 28. (Canceled)

29. (Previously presented) A method, comprising:

storing microcode on a computer readable medium external to a processor;

executing the microcode using the processor, wherein the processor includes a plurality of machine specific registers associated with at least two functional units of the processor; and

controlling one of the at least two functional units of the processor in response to executing the microcode by modifying a value of at least one bit included in one of the plurality of machine specific registers.

30. (Previously presented) The method of claim 29, wherein modifying a value of at least one bit included in one of the plurality of machine specific registers associated with one of the at least two functional units of the processor operates to affect the behavior of an other one of the at least two functional units of the processor.

31. (Previously presented) The method of claim 29, wherein a logical source register and a logical destination register for executing an instruction of the microcode are selected from the plurality of machine specific registers.

32. (Previously presented) The method of claim 29, wherein the at least two functional units are linked by a communication bus to a data control unit to fetch an instruction of the microcode from the computer readable medium external to a processor.

33. (Previously presented) The method of claim 29, wherein controlling one of the at least two functional units of the processor in response to executing the microcode further includes:

controlling a non-performance critical function.

34. (Previously presented) The method of claim 33, wherein the non-performance critical function is selected from the group consisting of:

cache flushing, cache invalidation, setting processor features, reading processor features, machine check handling, floating point calculations, processor diagnosis, architecture handling for backward compatibility, authentication, platform management interrupt, diagnostic functions and debug functions.

35. (Previously presented) An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:

storing microcode in firmware external to a processor;

executing the microcode by the processor;

updating one or more machine specific registers associated with a logic unit on the processor in response to the executing of the programmed code; and

controlling one or more functions of the logic unit on the processor based on a value stored in the one or more machine specific registers.

36. (Previously presented) The article of claim 35, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

moving a value from a general purpose register of the processor to the one or more machine specific registers.

37. (Previously presented) The article of claim 35, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

reprogramming the microcode in the firmware.

38. (Previously presented) An apparatus, comprising:

a first logic unit; and

at least two machine specific registers associated with the logic unit, the at least two machine specific registers to trigger processor hardware logic functions when a selected one of the at least two machine specific registers is updated in response to executing a microcode instruction fetched from a memory external to the processor.

39. (Previously presented) The apparatus of claim 38, further comprising:

a second logic unit associated with a selected one of the at least two machine specific registers.

40. (Previously presented) The apparatus of claim 39, wherein changing a value of at least one bit in a selected other one of the at least two machine specific registers affects the behavior of the second logic unit.

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